# A study of indentation annealing of (111) *p*-type single crystal silicon

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The indentation rosette size in (111) *p*-type Czochralski grown silicon was measured as a function of annealing temperature (450 to 1100°C), time (600 to 9300 sec) and indentation load (0.147 to 2.94 N). The indentations were made with the silicon surface immersed in an electrolytic solution containing Nal ions with concentrations in the range of  $10^{-5}$  to  $10^{-1}$  M l<sup>-1</sup>. The rosette size, 2*L*, was found to depend on the experimental variables as

$$\langle 2L \rangle = C t^{1/2} P^{1.15} \exp\left(\frac{-U}{kT}\right)$$

where C is a constant and t, T, P, and U are the annealing time, temperature, indentation load and energy, respectively, and k is Boltzmann's constant. The energy U has at least three different values depending on the annealing temperature interval and varies to a lesser extent on the indentation load.

### 1. Introduction

The mechanical properties of semiconductors are very important in the processing of these materials into shapes which are useful to the semiconductor industry. For example, single crystal semiconductors such as silicon and gallium arsenide are fabricated into wafers as the first step in the production of substrates for very large scale integrated (VLSI) circuits. This process involves the rubbing of diamond impregnated wheels or strings on the semiconductor surface, which is usually flooded by a fluid. The fluid removes the debris and the generated heat, lubricates the contacting surfaces, and may react chemically with the semiconductor. The abrasion deforms both surfaces of the semiconductor. This damage consists of cracks and plastic deformation, and the extent of this damage is a function of the abrasive and cutting wheel parameters, the loads and the fluids. This deformation is deleterious to the electrical properties of the semiconductor and it usually removed by mechanical and/or electrolytic polishing. Once electronic circuits are fabricated on the polished wafers, each device is removed by dicing the wafer with diamond-impregnated cut-off wheels. Abrasive damage is again generated at the outer perimeter of the electronic device.

Significant effort has been expended by researchers to characterize this damage so that the deformation parameters can be controlled and the resulting damage minimized. The importance attached to this research is justified, since microcracks may be the source of unpredicted brittle failure, and dislocations can contribute to failure as well as reduce the electrical efficiency of the device. Indentation has been used by a number of workers [1-5] as a relatively simple and straightforward test to determine deformation damage under prescribed experimental conditions. Indentation, a quasi-static test, produces a plastic zone when the diamond is impressed into the surface and produces cracks when the load on the diamond is released, in a manner analogous to cutting and dicing. When indentations are annealed, dislocation are known to propagate from the contact zone [6]. Generally, in semiconductor materials, dislocation double and single kink nucleation moves segments of dislocation half loops that intersect the surface. These loops have been detected in silicon by the double etching technique [7] and X-ray topography [8–10].

We have performed indentation tests on (111)*p*-type silicon, with the silicon surface immersed in a fluid containing varying concentrations of NaI. Electrolytic solutions have been shown to influence the hardness, crack length and residual stresses produced during indentation [11]. We have extended this work to include a study of annealed indentations in order to determine the load and temperature variation of dislocation dipole propagation. Annealing results in the propagation of dislocations from the vicinity of the indentation, when residual stresses are relieved. The experiments involve the etching of annealed indentations and the measuring of the rosette size as a function of the indentation parameters and annealing conditions.

#### 2. Experimental procedure

Indentations were made in the following way [12]. Single crystal silicon wafers, (111) *p*-type, 11 to  $12 \Omega$  cm, of 10.12 cm diameter and 0.54 mm thickness, were sectioned into quarters, etched in a 10 vol % hydrofluoric acid, and rinsed in deionized water for 120 sec. The quarters were immediately immersed in a



Figure 1 SEM micrograph of (111) p-type silicon indented under a load of 0.49 N in  $10^{-3} \text{ M} \text{ }^{1-1} \text{ NaI}$ , annealed at  $1100^{\circ} \text{ C}$ , for 7200 sec and etched in a dilute Sirtl solution.

solution which consisted of NaI dissolved in deionized water, with the NaI concentration varied from  $10^{-5}$  to  $10^{-1}$  M l<sup>-1</sup>. After soaking for 7200 sec, the silicon was indented with a pyramidal Vickers' diamond indenter with loads varying from 0.147 to 0.98 N. The diamond dwell time was 15 sec. Ten indentations were made at each load and the indentations formed a square array. The diamond was oriented so that the lines made by intersection of the pyramidal planes were perpendicular to  $\{110\}$ . After indentation, the sample was rinsed in deionized water and dried. Annealing was carried out in a three zone tube furnace in the temperature range of 450 to 1100°C for times as long as 9300 sec. Purified argon gas, supplied by a pressurized tank, was used to backfill the furnace during the anneal. At the end of the anneal, the samples were removed from the furnace, cooled, and etched in a dilute Sirtl solution for 25 sec. The indentation rosettes were observed by scanning electron microscopy (SEM) after vapour coating the surface with approximately 20 nm of gold. The rosette of each indentation was measured and the lengths were statistically analysed.

## 3. Results

The scanning electron micrograph in Fig. 1 shows an example of a typical annealed and etched indentation. In this case, the indenting load was 0.49 N; the NaI concentration was  $10^{-3}$  M I<sup>-1</sup>, and the annealing was carried out at 1100° C for 25 sec. This morphology is similar to that described in the literature [13]. Fig. 1 shows, as expected, dislocation etch pits which form the rosette, distributed along the  $\langle 1\bar{1}0 \rangle$  and  $\langle 10\bar{1} \rangle$  slip directions, and radial cracks that emanate from the corners of the pyramidal indentation. The spacing between etch pits gets larger away from the indentation and this indicates that the driving force to propagate dislocations is decreasing with distance. Although a few etch pits exist along  $\langle \bar{1}\bar{1}2 \rangle$ , the majority of them lie along  $\langle 1\bar{1}0 \rangle$  and  $\langle 10\bar{1} \rangle$ , and

occur in pairs. The formation of etch pit pairs is most likely due to double kink motion at elevated temperatures. In these experiments we did not observe dislocation rosettes below 200° C. This indicates that there is insufficient thermal energy below this temperature to activate dislocation propagation.

Fig. 2 shows examples of SEM micrographs of indentations made at a load of 0.245 N in a  $10^{-3}$  M  $1^{-1}$  NaI solution and annealed at 450°C (Fig. 2a), 500°C (Fig. 2b) and 1100°C (Fig. 2c). As can be seen, at 450°C the etch pits are clustered around the indentation and the figure shows the beginnings of the rosettes with dislocation propagation along the slip directions of  $\langle 1\bar{1}0 \rangle$  and  $\langle 10\bar{1} \rangle$ . As the annealing temperature is increased to 500°C, the rosette lengths increase, and finally, when the anneal temperature is 1100°C, the rosette arms become fully developed.

The indentation rosette length  $\langle 2L \rangle$ , of the largest rosette arms, varied with time and temperature of annealing and, with the concentration of NaI. Fig. 3 shows the average value and one standard deviation of  $\langle 2L \rangle$  against annealing time. In this case the indenting load was 0.245 N and the indents were carried out in  $10^{-3}$  M l<sup>-1</sup> NaI. The solid line indicates that the rosette lengths increase rapidly and appear to attain a steady state value after approximately 7200 sec.

Fig. 4 shows the variation of  $\langle 2L \rangle$  with concentration of NaI for an indentation load of 0.245 N and annealing time and temperature of 7200 sec and 1100° C, respectively. As shown in this figure,  $\langle 2L \rangle$  attains a maximum in the concentration range of  $10^{-3}$  to  $10^{-4}$  Ml<sup>-1</sup>. We have examined the variation of  $\langle 2L \rangle$  in this and other fluid environments, and these results will be the subject of another paper [14]. In this paper, we discuss the results in  $10^{-3}$  Ml<sup>-1</sup> NaI as a convenient and easily obtainable, uniform environment in which to perform indentations.

Fig. 5 shows the variation of  $\langle 2L \rangle$  over the temperature range of 450 to 1100° C for two indentation



*Figure 2* SEM micrograph of  $(1 \ 1) p$ -type silicon indented under a load of 0.245 N in  $10^{-3} \text{ M} \text{ }^{-1} \text{ NaI}$ , annealed at (a) 450, (b) 500 and (c) 1100° C for 7200 sec and etched in dilute Sirtl solution.

loads. This variation of  $\langle 2L \rangle$  against (T) has three stages. Rosettes are too small to be measured below 450° C, however their length increases rapidly up to approximately 700° C. The growth of the rosettes occurs from 700 to 900° C and, as expected, the rosettes increase in length when the load is increased from 0.147 to 0.245 N. Möller and Ewaldt [15] suggested that shrinkage as well as propagation determines dislocation mobility in the temperature range of ambient to approximately 0.7 of the melting point. It was proposed that the segments intersecting the surface are shorter than the line length, since image and line tension forces near the surface induce such processes.

The indentation load has a significant effect on the rosette size. Fig. 6 shows the variation of the rosette size as the load ranges from 0.147 to 2.94 N. These data are for indentations made in  $10^{-3}$  Ml<sup>-1</sup>NaI and annealed at 1100° C for 7200 sec. This figure shows that the slope is 0.87. This data is consistent with that of previous workers [16, 17]. For example, Tu and Yizhen [16] performed similar indentation at room temperature in (1 1) silicon using a load of 0.49 N.





They annealed the silicon at 947° C for 1800 sec. Hu [17] indented (1 1 1) silicon at 600° C. Both sets of data are also displayed in Fig. 6. While the environment under which their indentations were made is not given, both sets of data are consistent with the data of this paper. The results of Fig. 6 indicate that the rosette sizes are developed to the same length regardless of whether the indentations are performed at elevated temperatures or at room temperature and followed by an anneal.



Figure 3 Indentation rosette size (2L) against annealing time (min) at 950°C. (111) *p*-type silicon was indented in  $10^{-3}$  M  $^{1-1}$  Nal with a load of 0.245 N.



Figure 4 Indentation rosette size (2L) against the concentration of NaI solution. The indentations were made in  $(1 \ 1)$  p-type silicon with a load of 0.245 N, and annealed at 1100° C for 7200 sec.

#### 4. Discussion

The results of this study have shown that the dislocation rosette length varies with the NaI concentration of the water surrounding the pyramidal diamond during indentation, the indentation load, and annealing time and temperature. The rosettes develop as a result of residual stresses that are generated during indentation.

Fig. 7 shows the variation of  $\langle 2L \rangle$  against 1/T for three indentation loads. This data suggests an Arrhenius-type behaviour of the rosette size within each of four temperature ranges. The slope of the data within these temperature ranges is approximately constant and can be associated with U, an activation energy. These data are summarized in Table I, which shows the variation of  $\langle 2L \rangle$  within each temperature range for specific indentation loads. As can be seen, at temperatures of 450 to 500° C, U ranges from 0.34 to 0.31 eV as the indentation load varies from 0.147 to 0.98 N. The high temperature anneal of 925 to 1100° C shows a similar range of activation energies; these range from 0.33 to 0.44 eV. In the intermediate tem-

peratures, the activation energy is of the order of 0.1 to 0.2 eV in the temperature range of 500 to  $650^{\circ}$  C, and approximately zero from 650 to  $925^{\circ}$  C. It appears that the mechanism of dislocation dipole motion may be similar at the low and high temperatures with a transition region in the intermediate temperatures.

The data suggests the following dependence of  $\langle 2L \rangle$  on the indentation and annealing parameters,

$$\langle 2L \rangle = Ct^{1/2} P^{1.15} \exp\left(\frac{-U}{kT}\right)$$
 (1)

where C is a constant, t, P, U, and T are the annealing time, indentation load, activation energy for dislocation dipole propagation, and annealing temperature, respectively, and k is Boltzmann's constant. Hu [17] and Gridneva *et al.* [18] had suggested such a dependence of the rosette length on indentation load and temperature and these workers found that the exponent of indentation load varied from 0.2 to 0.33 with the activation energy equal to 2.2 to 2.3 eV. It is not possible at this time to trace the origin of the



Figure 5 Indentation rosette size (2L) against annealing temperature in (111) *p*-type silicon at 1100° C for 7200 sec with loads of  $\odot$ , 0.147 and  $\triangle$ , 0.245 N.



*Figure 6* Indentation rosette size (*L*) against indentation load. (•), Indentation of (1 1 1) *p*-type silicon was made at room temperature in  $10^{-3}$  moll<sup>-1</sup> NaI, and then annealed at 1100°C for 7200 sec. (present work). ( $\bigcirc$ ), Indentation at room temperature and annealed at 660°C for 1800 sec [16]. ( $\triangle$ ), Indented at 600°C [17].

differences between our values and those of these previous workers, although it is known that bulk doping and environmental influences can have a dramatic effect on dislocation velocities [19].

The shear stress that propagates dislocation dipoles may be deduced from a measurement of the etch pit spacing in an individual rosette leg.

The force between interacting dipoles has been

TABLE I Activation energy (eV) for rosette formation for (111) *p*-type silicon as a function of indentation load (N) at annealing temperature range (°C)

Annealing temperature (°C)	Activation energy (eV)			
	Indentat 0.147	ion load (N) 0.245	0.49	0.98
450-500	0.34	0.37	0.34	0.31
500-650	0.09	0.11	0.16	0.19
650925	0.0	0.0	0.0	0.0
925-1100	0.33	0.34	0.42	0.44

derived by Li [20] for edge dislocations as

$$F(x) = \frac{\mu b}{2\pi(1-\nu)} \left[ \frac{2}{x} - \frac{2x(x^2-y^2)}{(x^2+y^2)^2} \right]$$
(2)

Here  $\mu$  is the shear modulus of silicon (0.806 × 10<sup>11</sup> N m<sup>-2</sup>), **b** is the magnitude of the Burger's vector (0.383 × 10<sup>-10</sup> m),  $\nu$  is Possion's ratio (0.215 for  $\langle 1\bar{1}0 \rangle$ ) [21], x is the distance between each etch pit of the rosette leg and the first etch pit adjacent to the indentation, and y is the distance between neighbouring pairs of etch pits.

The shear stress can be obtained from F(x) since [22]:

$$\tau = -F/2\boldsymbol{b} \tag{3}$$

Since F(x) is known for various temperatures,  $\tau$  can be obtained for these same temperatures and Fig. 8 shows an example for the variation of  $\tau$  with 1/T for an indentation formed with a load of 0.245 N and annealed for 7200 sec. This figure shows a low and high temperature region. As expected, at low temperatures, high stresses are needed while at high temperatures the shear stress can be low to propagate the dipoles.



*Figure* 7 Indentation rosette size (2*L*) against the inverse of annealing temperature for (111) *p*-type silicon indented with loads of  $\bigcirc$ , 0.147;  $\triangle$ , 0.245 and  $\square$ , 0.49 N and annealed for 7200 sec.



Figure 8 Shear stress,  $\tau$  against 1/T. (111) *p*-type silicon was indented with a load of 0.245 N and annealed for 7200 sec.

#### 5. Conclusions

The following conclusions are reached from this study of annealing indentations (1 1 1) *p*-type single crystal silicon.

1. The indentation rosette size  $\langle 2L \rangle$  increases with annealing time and temperature, and indentation load. The indentation rosette size has three stages as the temperature increased.

2. The indentation rosette size increases with increasing indentation load. Our result is consistent with previous data of indentations performed at high temperatures. The mechanism for dislocation motion at high temperature is similar to that for dislocation motion during annealing indentations made at room temperature.

3. The concentration of NaI solution, in contact with silicon surface during indentation influenced the indentation rosette size. The maximum in rosette size is obtained in  $4 \times 10^{-4} M l^{-1}$ .

4. The rosette length  $\langle 2L \rangle$  depends on the experimental parameters as

$$\langle 2L \rangle = Ct^{1/2}P^{1.15} \exp\left(\frac{-U}{kT}\right)$$

where C is a constant and t, P, U, and T are the annealing time, indentation load, activation energy for dislocation dipole propagation and annealing temperature, respectively.

5. The activation energy for rosette length growth has four stages: U is 0.31 to 0.34 eV when  $450 < T < 500^{\circ}$  C, 0.1 to 0.2 eV when  $500 < T < 650^{\circ}$  C, 0.0 eV when  $650 < T < 925^{\circ}$  C, and 0.33 to 0.44 eV when  $925 < T < 1100^{\circ}$  C.

### Acknowledgement

This research was supported by the Solar Energy Research Institute under contract No. RL-7-06161-1. This support is gratefully acknowledged.

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Received 26 August 1986 and accepted 31 March 1987